What is claimed is:

1. A method of fabricating an integrated circuit device comprising:

forming an interlayer dielectric on an integrated circuit substrate;

forming a plurality of buried contacts in the interlayer dielectric;

forming an oxide layer on the interlayer dielectric;

forming an intaglio pattern in the oxide layer that exposes the plurality of buried contacts; and

forming a plurality of lower electrodes within a single opening in the intaglio pattern, the lower electrodes being in electrical contact with corresponding ones of the buried contacts.

2. The method of Claim 1 wherein forming a plurality of lower electrodes comprises forming the electrodes symmetrically in the intaglio pattern.

3. The method of Claim 1 wherein forming a plurality of lower electrodes comprises forming a plurality of semi-cylindrical electrodes.

4. The method of Claim 3 wherein the integrated circuit device comprises a ferroelectric memory device and wherein the forming a plurality of lower electrodes comprises forming a plurality of capacitors.

5. The method of Claim 4 wherein forming a plurality of capacitors comprises:

forming a lower electrode metal layer in the intaglio pattern;

forming a ferroelectric layer on the lower electrode metal layer;

forming an upper electrode metal layer on the ferroelectric layer; and then

patterning the formed lower electrode metal layer, ferroelectric layer and upper electrode metal layer to form the plurality of capacitors.

6. The method of Claim 4 wherein forming a plurality of capacitors comprises:

forming a lower electrode metal layer in the intaglio pattern;

patterning the lower electrode metal layer to form the plurality of lower electrodes;

forming a ferroelectric layer on the plurality of lower electrodes; and

forming upper electrodes on the ferroelectric layer.

7. The method of Claim 4 wherein forming an interlayer dielectric is preceded by forming transistors on the integrated circuit substrate and wherein forming a plurality of buried contacts comprises forming buried contacts electrically connected to respective ones of the transistors.

8. The method of Claim 1 wherein forming an intaglio pattern comprises removing a portion of the oxide layer to expose a portion of the interlayer dielectric and upper surfaces of the buried contacts.

9. The method of Claim 1 wherein forming an intaglio pattern comprises forming a multi-step intaglio pattern exposing upper surfaces of the buried contacts and part of an inner sidewall of the buried contacts and wherein forming a plurality of lower electrodes comprises forming a plurality of multi-step lower electrodes contacting the exposed upper surface and inner sidewall of corresponding ones of the buried contacts.

10. The method of Claim 9 wherein forming a multi-step intaglio pattern comprises:

removing a portion of the oxide layer to expose the upper surfaces of the buried contacts; and

removing a portion of the interlayer dielectric between the buried contacts to expose the part of the inner sidewall of the buried contacts.

11. The method of Claim 10 wherein the integrated circuit device comprises a ferroelectric memory device and wherein forming a plurality of lower electrodes comprises forming a plurality of capacitors.

12. The method of Claim 11 wherein forming a plurality of capacitors comprises:

forming a lower electrode metal layer in the intaglio pattern;

forming a ferroelectric layer on the lower electrode metal layer;

forming an upper electrode metal layer on the ferroelectric layer; and then

patterning the formed lower electrode metal layer, ferroelectric layer and upper electrode metal layer to form the plurality of capacitors.

13. The method of Claim 11 wherein forming a plurality of capacitors comprises:

forming a lower electrode metal layer in the intaglio pattern;

patterning the lower electrode metal layer to form the plurality of lower electrodes;

forming a ferroelectric layer on the plurality of lower electrodes; and

forming upper electrodes on the ferroelectric layer.

14. The method of Claim 11 wherein forming an interlayer dielectric is preceded by forming transistors on the integrated circuit substrate and wherein forming a plurality of buried contacts comprises forming buried contacts electrically connected to respective ones of the transistors.

15. The method of Claim 14 wherein forming an interlayer dielectric and forming a plurality of buried contacts comprises:

forming a first interlayer dielectric on the integrated circuit substrate including the transistors;

forming a bit line direct contact in the first interlayer dielectric and electrically contacting the transistors;

forming a bit line on the first interlayer dielectric and electrically contacting the bit line direct contact;

forming a second interlayer dielectric on the first interlayer dielectric including the bit line; and

forming the buried contacts in the first and second interlayer dielectric and electrically contacting corresponding ones of the transistors.

16. The method of Claim 15 wherein forming a plurality of lower electrodes comprises forming a plurality of semi-cylindrical electrodes symmetrically in the intaglio pattern.

17. An integrated circuit device comprising:

an integrated circuit substrate;

an interlayer dielectric on the integrated circuit substrate having a plurality of buried contacts therein;

an oxide layer on the interlayer dielectric;

an intaglio pattern in the oxide layer over the buried contacts; and

a plurality of lower electrodes within a single opening in the intaglio pattern, the

lower electrodes electrically contacting corresponding ones of the buried contacts.

18. The integrated circuit device of Claim 17 wherein the lower electrodes comprise semi-cylindrical lower electrodes symmetrically arranged in the intaglio pattern.

19. The integrated circuit device of Claim 17 wherein the integrated circuit device comprises a ferroelectric memory device and wherein the lower electrodes are lower electrodes of capacitors, the capacitors further comprising a ferroelectric layer on the lower electrodes and upper electrodes on the ferroelectric layers.

20. The integrated circuit device of Claim 19 wherein at least one of the lower electrodes comprises:

a horizontal electrode component contacting an upper surface of its corresponding buried contact; and

a vertical electrode component extending from the horizontal electrode component on a sidewall of the intaglio pattern.

21. The integrated circuit device of Claim 19 further comprising a plurality of transistors in the integrated circuit substrate and wherein the buried contacts electrically contact corresponding ones of the transistors.

22. The integrated circuit device of Claim 19 wherein the intaglio pattern comprises a multi-step intaglio pattern extending along upper surfaces of the buried contacts and a part of inner sidewalls of the buried contacts.

23. The integrated circuit device of Claim 22 wherein at least one of the lower electrodes comprises:

a first vertical electrode component extending along the part of the inner sidewall of its corresponding buried contact;

a horizontal electrode component extending from the first vertical electrode component along the upper surface of its corresponding buried contact; and

a second vertical electrode component extending from the horizontal electrode component along a sidewall of the multi-step intaglio pattern in the oxide layer.

24. The integrated circuit device of Claim 23 wherein the at least one of the lower electrodes further comprises a second horizontal electrode component extending inwardly from the first vertical electrode along a surface of the interlayer dielectric lower than a surface of the interlayer dielectric beyond the buried contacts.

25. The integrated circuit device of Claim 22 wherein the capacitors comprise semi-cylindrical capacitors symmetrically arranged in the intaglio pattern.

26. A method of fabricating a ferroelectric memory device including a semi-cylindrical capacitor comprising:

forming an oxide layer on an interlayer dielectric including a buried contact;

forming an intaglio pattern that exposes upper surfaces of at least two buried contacts;

forming at least two lower electrodes in contact with respective upper surfaces of the at least two buried contacts in the intaglio pattern; and

forming a ferroelectric layer and an upper electrode on the at least two lower electrodes.

27. A method of fabricating a ferroelectric memory device including semi-cylindrical capacitors, comprising:

forming an oxide layer on an interlayer dielectric including at least two buried contacts;

forming an intaglio pattern exposing the at least two buried contacts;

forming a lower-electrode metal layer contacting upper surfaces of the at least two buried contacts in the intaglio pattern;

forming a ferroelectric material layer and an upper-electrode metal layer sequentially in the intaglio pattern; and

patterning the upper-electrode metal layer, the ferroelectric material layer and the lower-electrode metal layer to form the semi-cylindrical capacitors in the intaglio pattern, each of the capacitors having a lower electrode contacting a corresponding one of the at least two buried contacts.

28. A method of fabricating a ferroelectric memory device including semi-cylindrical capacitors comprising:

forming an oxide layer on an interlayer dielectric including at least two buried contacts;

forming a two-step intaglio pattern exposing upper surfaces and a part of sidewalls of the at least two buried contacts;

forming at least two lower electrodes in contact with respective upper surfaces and sidewalls of the at least two buried contacts in the two-step intaglio pattern; and

forming a ferroelectric layer and an upper electrode sequentially on the lower electrodes.

29. A method of a fabricating a ferroelectric memory device including semi-cylindrical capacitors, comprising:

forming an oxide layer on an interlayer dielectric including at least two buried contacts;

forming a two-step intaglio pattern exposing the at least two buried contacts;

forming a lower-electrode metal layer contacting upper surfaces and sidewalls of the at least two buried contacts in the two-step intaglio pattern;

forming a ferroelectric material layer and an upper-electrode metal layer sequentially in the two-step intaglio pattern and on an upper surface of the oxide layer; and

patterning the upper-electrode metal layer, the ferroelectric material layer and the lower-electrode metal layer to form the semi-cylindrical capacitors including a lower electrode, a ferroelectric and an upper electrode, each of capacitors having a lower electrode contacting a corresponding one of the at least two buried contacts.

30. A ferroelectric memory device including semi-cylindrical capacitors, comprising:

an interlayer dielectric including at least two buried contacts;

an oxide layer formed on the interlayer dielectric;

an intaglio pattern exposing upper surfaces of the at least two buried contacts;

at least two lower electrodes formed in the intaglio pattern, each of the at least two lower electrodes being in contact with a corresponding one of the at least two buried contacts; and

a ferroelectric layer and an upper electrode sequentially formed on the lower electrodes.

31. A ferroelectric memory device including semi-cylindrical capacitors, comprising:

an interlayer dielectric including at least two buried contacts;

an oxide layer formed on the interlayer dielectric;

a two-step intaglio pattern exposing upper surfaces and a part of sidewalls of the at least two buried contacts;

at least two lower electrodes formed in the two-step intaglio pattern, each of the at least two lower electrodes being in contact with a corresponding one of the at least two buried contacts; and

a ferroelectric layer and an upper electrode sequentially formed on the lower electrodes.